SEMICONDUCTOR STRUCTURE HAVING A TEXTURED NITRIDE-BASED LAYER

REFERENCE TO PRIOR APPLICATION

[0001] The current application claims the benefit of co-pending U.S. Provisional Application No. 60/417,224, filed on October 9, 2002, which is hereby incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. TECHNICAL FIELD

[0002] The invention relates generally to nitride-based semiconductor structures, and more specifically, to a semiconductor structure that includes a textured nitride-based layer.

2. RELATED ART

[0003] Selective etching of nitride-based layers such as Aluminum Nitride (AlN) and Gallium Nitride (GaN) can be used in fabricating semiconductor devices. This etching relies on the difference between the respective etching rates for GaN and AlN. However, this approach does not allow for the selective etching of AlN layers that are widely used in nitride-based devices. Textured AlN layers and highly textured AlN boules can be produced by sputtering, Molecular Beam Epitaxy (MBE), or the like. Textured and epitaxial thin AlN layers have an etching rate that can be approximately two orders of magnitude higher than crystalline materials, making their manufacture more efficient. As a result, textured AlN layers have been applied to many solutions in electronic, electro-acoustic, and optoelectronic devices. However, to date, selective etching of a textured and/or epitaxial layer comprising, for example, AlN, GaN, InN, AlGaN, InGaN, or AlGaInN, deposited on an epitaxial layer comprising, for example, AlN, GaN, InN, AlGaN, InGaN, or AlGaInN, has not been used in the manufacture of semiconductor structures.

[0004] As a result, a need exists for a semiconductor structure that comprises a textured nitride-based layer formed above an epitaxially grown nitride-based layer.

SUMMARY OF THE INVENTION

[0005] The invention provides a semiconductor structure having a textured nitride-based layer formed above an epitaxially grown nitride-based layer. Specifically, under the present invention, a textured nitride-based layer is formed above an epitaxial layer (crystalline or amorphous) and a substrate in a semiconductor structure. In one embodiment, the textured nitride-based layer (such as textured AlN) is formed on a crystalline nitride layer. Various other layers and/or components can be included depending on the application for which the semiconductor structure will be used. The semiconductor structure can be used to form, for example, a field effect transistor or a light emitting device (e.g., light emitting diode, laser, etc.). Inclusion of the textured nitride-based layer can be used for designs that increase a lifetime and/or a reliability of the device, decrease a noise produced by the device, and/or make the device easier to manufacture.

[0006] A first aspect of the invention provides a semiconductor structure, comprising: a substrate; a first layer formed above the substrate; and a textured nitride layer formed on the first layer.

[0007] A second aspect of the invention provides a field effect transistor comprising: a substrate; an active layer formed above the substrate; a crystalline nitride layer formed above the active layer; and a textured nitride layer formed on the crystalline nitride layer.

[0008] A third aspect of the invention provides a light emitting device, comprising: a substrate; an n-type layer formed above the substrate; a light emitting structure formed above the n-type

layer; a p-type crystalline nitride layer formed above the light emitting structure; and a textured nitride layer formed on the crystalline nitride layer.

[0009] The illustrative aspects of the present invention are designed to solve the problems herein described and other problems not discussed, which are discoverable by a skilled artisan.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] These and other features of this invention will be more readily understood from the following detailed description of the various aspects of the invention taken in conjunction with the accompanying drawings in which:

[0011] FIG. 1 shows an illustrative semiconductor structure according to one embodiment of the invention;

[0012] FIG. 2 shows an illustrative semiconductor structure according to another embodiment of the invention;

[0013] FIG. 3 shows an illustrative semiconductor structure according to still another embodiment of the invention;

[0014] FIG. 4 shows an illustrative semiconductor structure having a patterned textured nitride layer according to one embodiment of the invention;

[0015] FIG. 5 shows a top view of the structure in FIG. 4;

[0016] FIG. 6 shows an illustrative semiconductor structure having a patterned textured nitride layer according to another embodiment of the invention;

[0017] FIG. 7 shows an illustrative field effect transistor according to one embodiment of the invention;

[0018] FIG. 8 shows an illustrative field effect transistor according to another embodiment of the invention;

[0019] FIG. 9 shows an illustrative field effect transistor according to still another embodiment of the invention;

[0020] FIG. 10 shows an illustrative field effect transistor according to yet another embodiment of the invention;

[0021] FIG. 11 shows an illustrative field effect transistor according to yet another embodiment of the invention;

[0022] FIG. 12 shows an illustrative light emitting device according to one embodiment of the invention; and

[0023] FIG. 13 shows an illustrative light emitting device according to another embodiment of the invention.

[0024] It is noted that the drawings of the invention are not to scale. The drawings are intended to depict only typical aspects of the invention, and therefore should not be considered as limiting the scope of the invention. In the drawings, like numbering represents like elements between the drawings.

DETAILED DESCRIPTION OF THE INVENTION

[0025] It is understood that for the purposes of the present invention, Al means Aluminum, In means Indium, Ga means Gallium, and N means Nitrogen.

[0026] As indicated above, the invention provides a semiconductor structure having a textured nitride-based layer formed above an epitaxially grown nitride-based layer. Specifically, under the present invention, a textured nitride-based layer is formed above an epitaxial layer (crystalline or amorphous) and a substrate in a semiconductor structure. In one embodiment, the textured nitride-based layer (such as textured AlN) is formed on a crystalline nitride layer. Various other layers and/or components can be included depending on the application for which

the semiconductor structure will be used. The semiconductor structure can be used to form, for example, a field effect transistor or a light emitting device (e.g., light emitting diode, laser, etc.). Inclusion of the textured nitride-based layer can be used for designs that increase a lifetime and/or a reliability of the device, decrease a noise produced by the device, and/or make the device easier to manufacture.

[0027] Turning to the drawings, FIG. 1 shows an illustrative semiconductor structure 10 according to one embodiment of the invention. Semiconductor structure 10 is shown including a substrate 12, a first layer 14 formed over substrate 12, and a textured nitride layer 16 formed over first layer 14. Substrate 12 can comprise any material known in the art including, for example, sapphire, silicon carbide, aluminum nitride, gallium nitride, zinc oxide, lithium gallate, lithium niobate, diamond, silicon, or the like. First layer 14 can comprise, for example, a crystalline or epitaxial nitride layer. To this extent, first layer 14 and/or textured nitride layer 16 can comprise, for example, AlN, GaN, InN, AlGaN, InGaN, AlGaInN, or the like. It is understood that throughout the drawings, each layer shown can be deposited directly on the lower layer or one or more additional layers can be formed between the two layers. For example, a buffer layer can be included between substrate 12 and first layer 14.

[0028] Semiconductor structure 10 can be configured to operate as any type of semiconductor device, including for example, a power switching device, a microwave device, an optoelectronic device, and an acousto-optic device. Examples of these devices include a photodetector, a field effect transistor, a gated bipolar junction transistor, a gate hot electron transistor, a gated heterostructure bipolar junction transistor, a gas sensor, a liquid sensor, a pressure sensor, a multi-function sensor of both pressure and temperature, a light emitting diode, a laser, and the like. To this extent, semiconductor structure 10 can include one or more additional layers/structures formed between substrate 12 and first layer 14, between first layer 14 and

textured nitride layer 16, and/or above textured nitride layer 16. Further, each layer can be formed over all or only a portion of a lower layer, can vary in thickness, and can be formed into any pattern that provides the desired functionality for the semiconductor device. Each layer can be deposited and/or patterned using any solution now known or later developed. For example, textured nitride layer 16 can be formed using MBE and/or patterned using selective etching to remove a portion of textured nitride layer 16.

[0029] As noted, semiconductor structure 10 can include one or more additional layers. For example, FIG. 2 shows semiconductor structure 10 having a second layer 18 formed above textured nitride layer 16. In one embodiment, second layer 18 can comprise a dielectric layer or a composite dielectric layer comprising silicon dioxide, silicon nitride, or the like. In this case, second layer 18 can passivate one or more layers formed below second layer 18, e.g., textured nitride layer 16. In an alternative embodiment, second layer 18 can comprise a metal layer. In this embodiment, the metal layer can serve as a gate of a field effect transistor, such as a Heterostructure Field Effect Transistor (HFET) or a Metal Oxide Heterostructure Field Effect Transistor (MOSHFET).

[0030] Additionally, semiconductor structure 10 can include one or more layers formed between substrate 12 and first layer 14 and/or between first layer 14 and textured nitride layer 16. For example, FIG. 3 shows semiconductor structure 10 having a buffer layer 20 and a third layer 22 formed between substrate 12 and first layer 14. Buffer layer 20 and third layer 22 can each comprise, for example, any combination of AlN, GaN, AlGaN, AlGaInN, or the like, and third layer 22 could have a graded composition. Buffer layer 20 provides a buffer between substrate 12 and third layer 22. It is understood that buffer layer 20 could be included without third layer 22. In this case, buffer layer 20 would provide a buffer between substrate 12 and first layer 14. Third layer 22 can comprise an active layer or the like that provides functionality for

semiconductor structure 10. Third layer 22 can provide improved localization of carriers in the channel, and can be included as part of a device such as a Double Heterostructure Field Effect Transistor.

[0031] As noted previously, one or more layers of semiconductor structure 10 could be formed into a pattern. The pattern could be used to form a photonic crystal, incorporated as part of a mechanical electronic monolithic structure, form a passive element for a monolithic microwave integrated circuit (e.g., resistor, capacitor, inductor, transmission line, interconnect, etc.), or the like. For example, FIG. 4 shows a side view and FIG. 5 shows a top view of semiconductor structure 10 in which textured nitride layer 16 has been formed into a stripe pattern that comprises a set of stripes 24A-D. Set of stripes 24A-D can be formed in the construction of a striped light emitting diode (LED) structure that can be used to reduce current crowding effects in an LED. It is understood that additional layers can also be formed into a pattern. For example, textured nitride layer 16 and second layer 18 shown in FIG. 2 both could be formed into the set of stripes 24A-D, with second layer 18 formed above textured nitride layer 16 on each stripe 24A-D. Alternatively, FIG. 6 shows a top view of semiconductor structure 10 in which textured nitride layer 16 has been formed into a circle pattern that comprises a set of circles 26A-D. Set of circles 26A-D can be used, for example, in fabricating an array of LEDs or laser diodes. It is understood that the embodiments shown are only illustrative of the various patterns that can be formed, numerous alternative patterns can be formed under the invention.

[0032] Semiconductor structure 10 can be configured to operate as any type of semiconductor device. For example, FIG. 7 shows a semiconductor structure configured to operate as a field effect transistor (FET) 30. To this extent, field effect transistor 30 is shown including a substrate 12, buffer layer 20, and active layer 22 as discussed above with reference to FIG. 3. Further, field effect transistor 30 includes a source contact 32, drain contact 34, and gate contact 36

formed above textured nitride layer 16. In this configuration, first layer 14 and textured nitride layer 16 form a gate barrier structure 38 between active layer 22 and contacts 32, 34, 36. First layer 14 can comprise, for example, a crystalline nitride layer. It is understood that source contact 32, drain contact 34, and gate contact 36 can be located on field effect transistor 30 in any manner. For example, gate contact 36 can be located closer to source contact 32 than drain contact 34.

[0033] Various alternative configurations for field effect transistor 30 are possible. For example, FIG. 8 shows a field effect transistor 30A in which textured nitride layer 16A only covers a portion of first layer 14 to form a gate barrier structure 40. In this configuration, gate contact 36A is formed on first layer 14, and source contact 32 and gate contact 34 are formed on textured nitride layer 16A. Alternatively, FIG. 9 shows a field effect transistor 30B in which source contact 32B and drain contact 34B are formed on first layer 14, while gate contact 36B is formed on textured nitride layer 16B. As shown, textured nitride layer 16B is adjacent to and contacts both source contact 32B and drain contact 34B, and has a narrower width below gate contact 36B to form a recessed gate structure. It is understood that various additional alternatives to the embodiments shown are also possible. For example, all three contacts 32, 34, 36 could be formed on first layer 14 with textured nitride layer 16 being formed adjacent each contact. Further, all three contacts 32, 34, 36 could be formed on textured nitride layer 16, and textured nitride layer 16 can form a recessed gate structure under gate contact 36B.

[0034] Additionally, field effect transistor 30 can include one or more additional layers. For example, FIG. 10 shows a field effect transistor 30C similar to field effect transistor 30B shown and discussed in FIG. 9, except that field effect transistor 30C includes a passivating layer 18C. Passivating layer 18C can comprise, for example, a dielectric layer comprised of silicon dioxide, silicon nitride, or the like. Alternatively, FIG. 11 shows a field effect transistor 30D in which

passivating layer 18D is formed between textured nitride layer 16D and gate contact 32D, thereby forming a dielectric barrier between textured nitride layer 16D and gate contact 32D.

[0035] The semiconductor structure can also be configured to operate as a light emitting device. For example, FIG. 12 shows a light emitting device 42 that includes a substrate 12, a first layer 14, and a textured nitride layer 16. Light emitting device 42 also includes a first structure 43, a light emitting (active) structure 44, and a contact 46. As shown, textured nitride layer 16 is formed above a portion or a section of first layer 14, and contact 46 is formed above the remainder of first layer 14, adjacent to textured nitride layer 16. In an alternative embodiment shown in FIG. 13, contact 46A is formed above only a portion of first layer 14 that is not covered by textured nitride layer 16, and is adjacent to only a portion of textured nitride layer 16. In either case, first structure 43 can comprise one or more n-type layers, and first layer 14 and/or contact 46 can comprise p-type layers. Light emitting structure 44 can comprise one or more layers configured to generate light when light emitting device 42 is in operation. For example, light emitting structure 44 can comprise one or more layers that emit light of a desired frequency (e.g., in a light emitting diode), or light of a particular frequency that is also aligned in a particular manner (e.g., in a laser).

[0036] The foregoing description of various embodiments of the invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed, and obviously, many modifications and variations are possible. Such modifications and variations that may be apparent to a person skilled in the art are intended to be included within the scope of the invention as defined by the accompanying claims.